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Failure Assessment Software for Circuit Card Assemblies

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SUMMARY & CONCLUSIONS

Up-front failure analysis of circuit card assembly designs can dramatically reduce cost of ownership, increase product reliability, and thus reduce risks. In this paper, the design process for electronic products is discussed in terms of failure assessment activity. Information resources necessary to support the failure assessment activity are discussed. Finally, the effectiveness of failure assessment software is demonstrated by analyzing circuit card assemblies (CCAs) from a military radio control module using the calcePWA software (Ref. 1 and 2) developed by the CALCE Electronic Products and Systems Center (EPSC) at the University of Maryland.

1. *THE ELECTRONIC DESIGN PROCESS*

The electronics industry spends considerable effort in the development of sophisticated tools for schematic capture, component placement, electrical simulation, and routing. This support comes from the Electronic Design Automation (EDA) Industry. Unfortunately, design automation initiatives regularly ignore or provide only cursory attention to the mechanical design aspects of the electronic design process (Ref 3).

In examining the electronic design process, it is clear that a central component is the ability to examine the risks. With the advent of simulation software, electronic product development is moving from the design-build-test mentality to a spiral development model (Ref. 4). The spiral model consists of four key phases through which the development process cycles. These phases include:

1. Development and verification phase;
2. Plan phase;
3. Object, alternatives, and constraints phase; and
4. Risk evaluation phase.

For hardware development process, the product moves from concept, requirements planning, to risk assessment, to requirements definition, to development planning, to risk assessment, and so on. The cyclic process always returns to risk analysis. Key components to risk assessment include technology risk, market risk, and supply chain risk. Obviously, cost is the deciding factor in the risk assessment process, but failure assessment capabilities are critical in evaluating supply chain and technology risk.

To best impact the product, the failure assessment should be performed in the early design (concept phase) and carried into the detailed design phase. The benefits of failure assessment include:

identification of design flaws;
identification of weak or problem parts;
identification of destruction limits;
identification of wearout limits; and
estimation of failure free operating periods.

Boeing Commercial Airplane Group has estimated that up to 40% reduction in cost and weight could be achieved if reliability assessment could be integrated into the design phase (Ref. 5). A flowchart of how failure assessment fits into the electronic design process is presented in Figure 1.

1.1 *Outputs and Benefits of the Failure Assessment Process*

The first and primary output of the failure assessment process is the determination of failure locations, types, and severity. This requires a scientific understanding of how materials react to loads, which allows for the development of algorithms and analytic models that can be used to predict failure. A related function of the failure assessment process is the ability to predict defects introduced during the manufacturing process.

Cost reduction can be achieved by reducing product qualification testing from understanding how a product will fail. Failure assessment is critical in this regard since higher than normal stress conditions are needed to fail the product in a short period of time. Failure assessment is needed to determine how the product will react under these high load conditions and to map the outcome of accelerated test conditions to product performance in the actual use condition. Failure assessment can be used to help determine the test

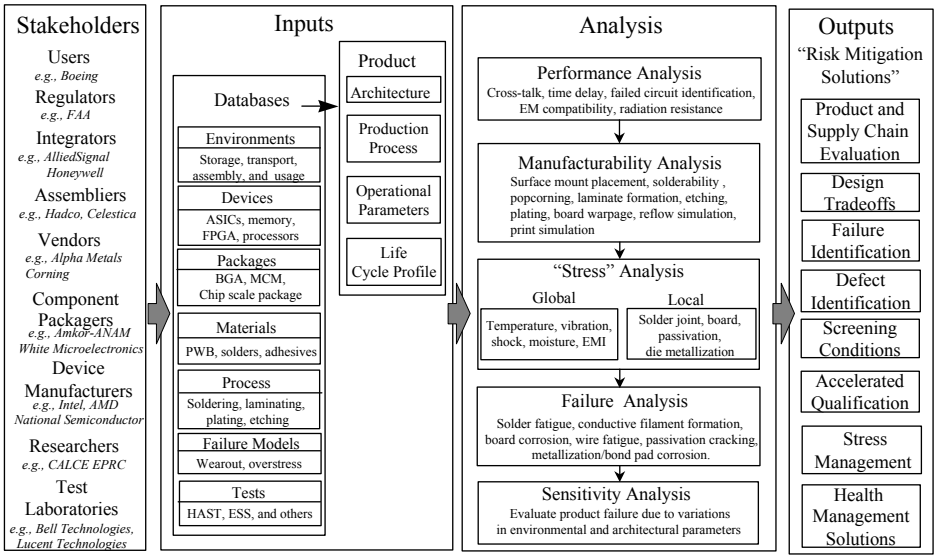


Figure 1. Flow chart for failure assessment in electronic hardware development

conditions and product fixturing necessary to excite only relevant failures. In addition, it can be used to warn of failures that may occur only as a result of the accelerated test conditions.

Along with product qualification, failure assessment is critical to product screening. Screens are used to remove products that fail earlier than expected due to manufacturing defects.

Screening involves examining the product during or after manufacture to find the types, locations, and severity of flaws introduced from the manufacturing process. Screens can be carried out by product inspection and/or stress-based screening methods. To apply a stress, screening is necessary to know what failures result from defects in the product and how the application of external loads can precipitate failure of flawed products. Failure assessment helps in this area by providing time-to-failure estimates based on material, geometry, and load conditions. A manufacturing flaw may be represented and an inappropriate geometry and/or a changed material property. Applying this information to the failure assessment process allows us to determine if a stress-based screen is viable.

Information regarding the type, location, and severity of failures and defects allows the product and supply chain to be evaluated. For example, the use of alternative parts from different suppliers may be evaluated to determine whether the change allows the product to meet its requirement. The use of plastic encapsulated microcircuits as opposed to ceramic packages is an example of such a process.

Failure assessment also provides a basis for performing stress management. Stress management solutions can be evaluated in terms of their effectiveness in reducing harmful loads and increasing the useful life of a product. For instance, the response of the product to various levels of vibration can be used to determine the amount of damping required to protect the equipment.

Finally, failure assessment allows for the development of guidelines for equipment monitoring and devices to provide early warnings for imminent equipment failure. By understanding, the type, location, and severity of failures in the electronic product, stresses may be monitored allowing for estimates of useful remaining life. In an alternative approach, devices, such as fuses, may be developed based on expected failures. Under field loading conditions, these fuse devices would be calibrated to fail before any expected product failure, thus becoming an integral part of an early warning system. Since the material, architecture, and use conditions of an electronic product are generally unique, the design of the fuse or fuses requires a failure assessment of the product. Once again, the failure assessment process aids in this effort.

1.2 *Stress Analyses for Failure Assessment*

An important part of the failure assessment process involves simulating load states during the transport, operation, and storage of an electronic product. In general loads which affect product life may be electro-magnetic, mechanical loads (dynamic or static), chemical, temperature, and radiation.

In order to determine the load level at potential failure sites, it is

necessary to perform one or more levels of structural or load analysis. Since many predominate failures in electronics involve mechanical failures at the interface of joined materials (i.e. solder joints, plated though holes), stress evaluation of an electronic product should include temperature and vibration analysis. In addition, corrosion and metal migration in electronic products is associated with moisture. Thus, it is necessary to estimate the level of moisture in the electronic products. Other simulation methods may be necessary to determine the amount of caustic chemicals due to manufacturing and environment. In addition, the level of harmful radiation must also be determined.

The stress states which are monitored depend on the failures which are being assessed. Some common stress measurements for components on printed wiring boards are provided in Table 1.

Table 1 Key Component Stress Parameters

Maximum Case Temperature
Minimum Case Temperature
Maximum Device Junction Temperature
Minimum Device Junction Temperature
Maximum Substrate Temperature
Minimum Substrate Temperature
Maximum Curvature under Component
Maximum Displacement under Component
Moisture content of printed wiring board
Voltage bias between adjacent metallization regions

1.3 *Inputs for Failure Assessment*

Efficient risk assessment and mitigation requires an infrastructure of up-to-date failure mechanisms, materials, and environment/test stress libraries. The following sections describe the libraries required to perform a successful failure assessment.

1.3.1 *Environment Library*

Electronics design requires descriptions of the application environment in which the product will be used. An environment library should include storage, transportation, and use environments. These environments are used in performing stress analysis and reliability assessment. Nine standard usage environments are included with the software and are shown in Table 2. Users should also be able to create and define their own environments. Key environmental parameters included in the library are included in Table 3.

Table 2. Key environments

Office	Automotive Under Hood
Consumer	Military Ground & Ship
Telecommunications	Industrial Motors
Commercial Avionics	Space (GEO)
Military Avionics	

Table 3. Key environmental parameters

Maximum temperature	# of humidity cycles/year
Minimum temperature	Vibration mode
Average temperature	Vibration wave form
Temperature cycle	Acceleration PSD
# temperature cycles/year	Time of pulse
Maximum relative humidity	Maximum G-force
Minimum relative humidity	Maximum acceleration
Average relative humidity	Ionic concentration
	Industrial gas concentration

1.3.2 *Materials Library*

Knowledge of material properties is a critical element of the failure assessment process. Materials can be organized by the usage categories, such as those shown in Table 4.

Table 4. Key materials

Attach materials	PWB materials
Component materials	Solder materials
Metallization materials	
Lead materials	

The key material parameters are presented in Table 5.

Table 5 Key material parameters

Elastic modulus	Thermal conductivity
Shear modulus	Specific heat
Yield strength	Electrical conductivity
Ultimate tensile strength	Chemical valence
Coefficient of thermal expansion	Atomic weight
Poisson's ratio	Density
Fatigue coefficient	Permeation constant
Fatigue exponent	

1.3.3 *Part Definition, Architecture and Geometry Libraries*

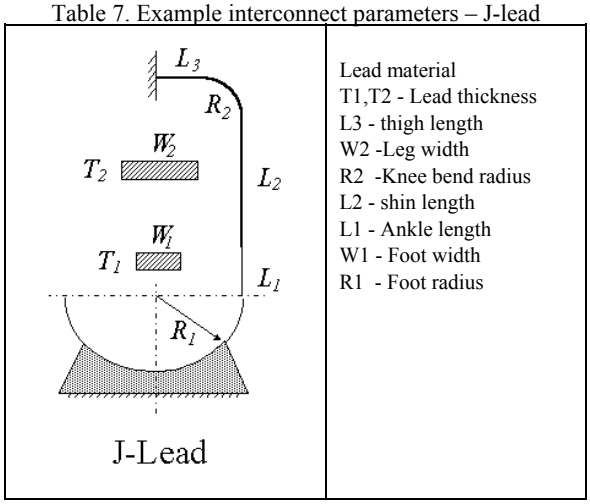
A part (e.g., integrated circuit) is a marriage of a package and device. The architecture of a part is based on the package format. There is a multitude of parts produced by various electronic component suppliers; however, there are relatively few package geometries. The distinction between the part and package is important since multiple parts have identical package architectures. A package may be represented by a set of geometric and information parameters. The number and types of parameters are defined by package format. There are several common parameters that may be applied to almost all package formats. These parameters are included in Table 6.

Table 6. Common package parameters

Package Format	Maximum Power Dissipation
Package Length	Case Material
Package Width	Interconnect Format
Package Thickness	Interconnect Pitch
Package Weight	Number of interconnects
Maximum Rated Temperature	

A separate but closely related structure is the interconnect between the component (i.e., part) to the board. The choice of package format typically limits the interconnect format and geometry. As in the package definition, the geometric parameters are defined by the interconnect format. An example of interconnect parameters for a J-lead is presented in Table 7.

Table 7. Example interconnect parameters – J-lead



Lead material
T1,T2 - Lead thickness
L3 - thigh length
W2 -Leg width
R2 -Knee bend radius
L2 - shin length
L1 - Ankle length
W1 - Foot width
R1 - Foot radius

In addition to material and geometry information associated with a part, it is also necessary to track geometry and material information associated with the fabrication and assembly process. For example, the shape, area, and height of surface-mount lead-to-board interconnect is required to determine its resistance to cyclic loading damage.

1.3.4 *Failure Model Library*

The heart of the failure assessment process is the failure model library. The failure model library is a collection for known algorithms and documentation of known failures. A failure model entry contains the algorithms and documentation necessary to estimate time to failure at a specific site due to a specific failure mechanism. Failure models express the time to failure for each mechanism based on geometry attributes, material properties, and environmental/operational stress levels. In some cases, models provide internal algorithms that are used to calculate local stress conditions from global stress conditions arising from the environmental/operational stress levels. The sources, assumptions, limitations, and validation histories for each model are also provided. Example failure mechanisms are listed in Table 8.

Table 8. Example failure mechanisms

J-lead solder thermal fatigue	Conductive filament formation
Gullwing solder thermal fatigue	PWB shock failure
BGA solder thermal fatigue	Metallization corrosion
Gullwing vibration fatigue	J-lead shock failure
J-lead vibration fatigue	Gullwing Shock Failure
BGA vibration fatigue	BGA shock failure
DIP vibration fatigue	PGA lead shock failure
PGA vibration fatigue	DIP lead shock failure
PTH Barrel Fatigue	

In order to impact product reliability, failure assessment must be applied as early as possible in the design process. This is accomplished by using software which implements the features discussed above. The calcePWA software (Ref. 1 and 2) developed by the University of Maryland has all of the features necessary to perform failure assessment for CCAs. Figure 2 depicts where calcePWA has been incorporated into the electronic design process. In this figure, failure assessment for a PWA design is shown to begin at design concept when components are being selected, the board material and geometry is being developed, and the component placement is in flux. Environment and usage conditions must also be considered during this stage. Once in place, the failure assessment model grows with the design. This allows designers to consider the effects of design decisions on reliability as the product design matures.

2. *EXAMPLE USAGE*

To illustrate how failure assessment software is applied to electronic design, a case study is presented for electronics in a military system. In this study, the calcePWA software (Ref. 1 and 2) was used to determine possible failure mechanisms due to operating and environmental conditions on three CCAs in a control module of a military radio. Subsequent physical testing was performed to validate the failure assessment results. A photo of the control module can be seen in Figure 3.

The control module consists of three circuit boards, an aluminum frame and two aluminum backplanes. Each circuit board has six layers and contains commercial and military components. These components are ceramic and plastic and use surface-mount and through-hole-attachment technology. The three boards are encased in an aluminum frame with CCAs #1 and #3 having a bonded aluminum backplane. The three CCAs contained 50 microcircuits, seven connectors, 22 inductors, 44 semiconductors, 241 capacitors, 222 resistors, and four miscellaneous parts. Despite differences in layout, some parts and electrical functions of the CCAs were very similar. The bare boards were constructed of BT laminates and contained six signal/power/ground planes. The total thickness of CCAs #1 and #3 were approximately 37 mils and the thickness of CCA #2 was approximately 58 mils.

To facilitate import of the data, electronic design files generated by Zuken-Recal design system were imported through the calcePWA import facility. Further data entry and manipulation was required after the initial import process since the electronic design system did not carry all of the information necessary to

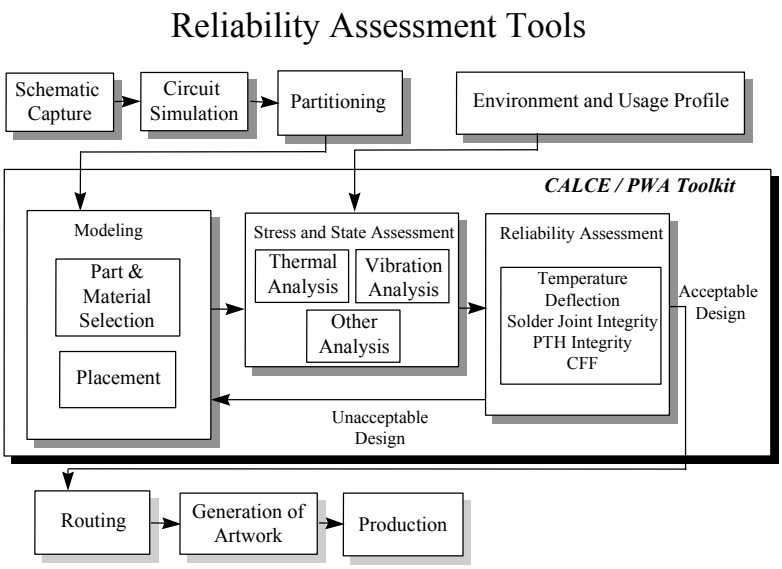


Figure 2 Role of failure assessment in the design of electronic products

make a failure assessment. For example, detailed lead geometry, lead materials, package materials, detailed package sizes, laminate materials, and laminate thicknesses were not specified. At first, import default values were used for the missing information. These values were updated over the course of the study.

Figure 3 Military Radio and the Control Module

2.1 *Environmental Conditions*

While the model was being developed, a test plan was constructed to allow a one-to-one comparison of test data and analysis results data. Based on the radio's anticipated military environment, temperature and vibration loads were selected to induce failures. The level and duration of the vibration test were based on the product qualification test that included random vibration at $0.04g^2$/Hz, between 20 to 2000Hz, for four hours. The temperature test consisted of cycling between -50°C and 95°C with 15-minute dwells at the temperature extremes. A complete temperature cycle lasted approximately two hours.

2.2 *Vibration Analysis*

In order to determine the local stresses within each CCA, a vibration analysis of each CCA was performed using the calcePWA. Inputs to the software included a detailed set of boundary conditions, the applied Power Spectral Density (PSD) curve from the test specifications, and a damping factor of 0.05.

From examining the assembly, it was observed that CCAs #1 and #3 were supported completely along their edges. In addition, the support appears to be fairly rigid. As a result, the first vibration model defined the outer edges as clamped supports. A more conservative approximation was later used, which changed the clamped supports to simple supports. Several screws supported CCA #2, and simple point supports were used to conservatively approximate their support. CCAs #1 and #3 each weighed approximately one eighth of a pound, including the aluminum backplane, and had a rigidity of approximately 185 lb-in. CCA #2 weighed less than a tenth of a pound and had a rigidity of approximately 77 lb-in. Figure 4 depicts the screen captured image of the boundary conditions for CCA #3.

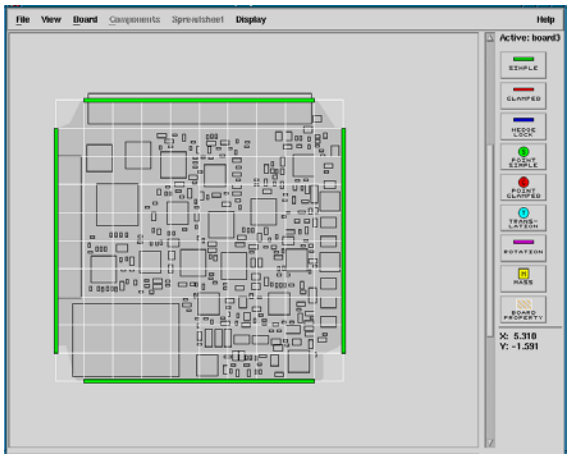


Figure 4 Support Conditions of for CCA #3

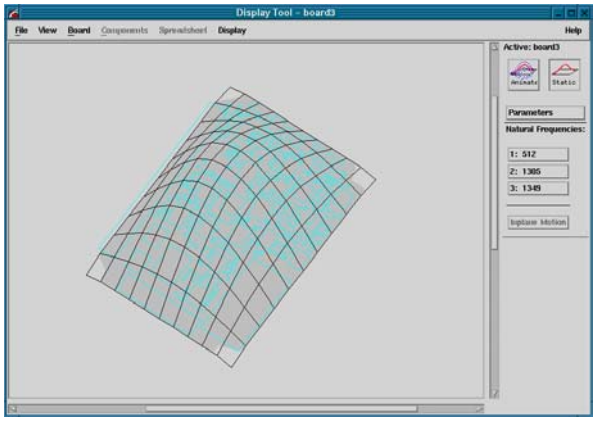


Figure 5 First fundamental mode shape for CCA #3

The calcePWA software calculates the first three natural frequencies and mode shapes for the analyzed CCA. The analysis results indicated that the first mode frequency of each board was above 500 Hz. Figure 5 depicts the first mode shape as well as the three calculated frequencies for CCA #3. In addition to the mode shapes, the software also calculates the one-sigma board deflection. This information is presented graphically in the calcePWA software.

2.3 *Thermal Analysis*

A thermal analysis was performed on each CCA to identify component temperatures and the thermal distribution throughout each board due to component power dissipation and the effectiveness of the cooling paths. Inputs to the thermal-analysis module included component, printed wiring board (PWB), and cooling data. Package dimensions, power dissipation, junction-to-case thermal resistance, and material properties were taken from the manufacturer's data sheets.

In developing the thermal analysis models, the metal housing which supported each board along its edges was assumed to be the primary heat sink. Figure 6 depicts the applied thermal boundary conditions for one of the thermal analysis runs which was performed on CCA #3. This boundary condition was used for each of the circuit cards assemblies under investigation.

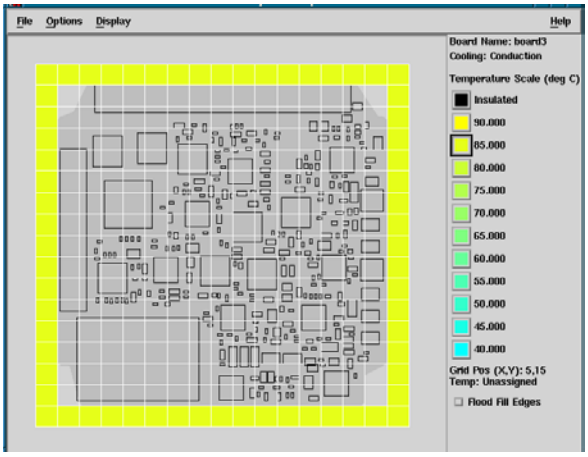


Figure 6 Thermal Boundary Conditions for CCA #3

Due to the relatively small heat dissipation of the components on each card, the board and component temperatures were only slightly higher than the applied boundary condition temperature. Figure 7 depicts the component temperature for CCA #3. Discussions with the radio module vendor confirmed that the CCA temperatures would closely match the applied boundary conditions. This observation simplified the failure assessment process.

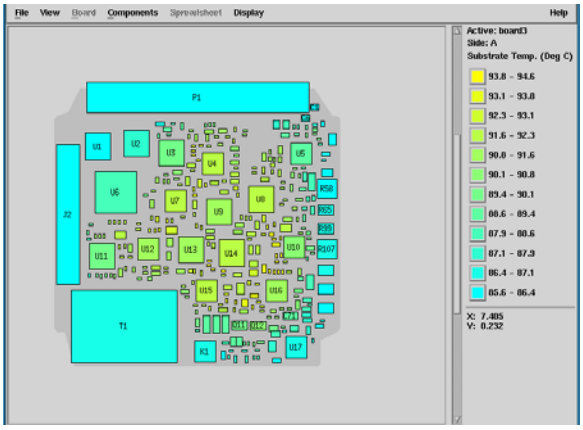


Figure 7 Component Temperatures for CCA#3

2.4 *Failure Assessment*

The failure assessment module of the calcePWA software was used to analyze potential failure sites on each of the CCAs. Failure mechanisms that were assessed included solder-joint and lead fatigue, via barrel fatigue, and metal migration. The thermal and vibration analysis results along with other

operational and environmental information were used in the failure assessment process.

2.4.1 *PWB Failure Assessment*

The plated-through hole (PTH) barrel fatigue model (Ref. 6) predicts the fatigue life of PTH plating when subjected to repeated thermal cycles. This life estimation is based on the engineering principle that failures result from the mismatch in the coefficient of thermal expansion (CTE) between the plating material and the board material in the out-of-plane (thickness) direction of the PWB, thus producing stress between the layers and the plating material. To achieve a conservative solution, only the worst case PTH was modeled. The PTH model, depicted in Figure 8, was based on the planned physical tests evaluated for a ΔT of 145°C. The long life predicted by the model indicates that failure due to barrel fatigue did not pose a significant problem.

The conductive filament formation model (Ref. 7) predicts the time required for a metal filament to migrate between electrically biased conductors. This model considers the moisture content, conductor geometry and spacing, and voltage bias when calculating the time to failure. The analysis of the control model CCAs and the environmental conditions indicated that conductive filament formation did not pose a substantial risk.

2.4.2 *Interconnect Failure Assessment*

Component interconnect failure is one of the primary wearout failures observed in circuit card assemblies. Interconnect failures are most typically due to fatigue. To assess the interconnect failures, first order models including modified versions of Englemaier's leaded and leadless thermal fatigue (Ref. 8) and Steinberg's random vibration fatigue model (Ref. 9) were employed. Inputs for the interconnect failure analysis models include the component position, component size, interconnection format, interconnection material, and component material. Board curvature under the component, as well as component case and board temperatures, are extracted from the thermal and vibration analysis results. Other information such as temperature cycle dwell times and frequency of vibration exposure is required to perform the analysis.

The random vibration induced fatigue failure model was applied against each of the three circuit cards with an excitation level 0.04 g^2/Hz. The results of the vibration induced fatigue model evaluation indicated that no significant problems existed for a vibration loading of 0.04 g^2/Hz.

The thermal induced fatigue model was applied for each of the three circuit cards with an imposed ΔT of 145°C. The results exposed a potential failure problem for certain parts on CCA #2 and CCA #3. Figure 9 provides a graphical depiction of thermal fatigue failure assessment results for CCA #3. From this figure, it can be seen that eight 20-pin leadless chip carriers (LCCs) have life estimates below 900 temperature cycles. On CCA #2, the failure assessment analysis indicated that one LCC would have a life below 1000 temperature cycles. Based on the projected field service environment, these results indicate that failures will occur in less than seven years. Other packages have greater life times and should not influence the CCA's life.

3. *EXPERIMENTAL TEST RESULTS*

Physical testing was performed to verify the software results. The experimental program incorporated temperature cycling and random vibration tests. The temperature cycling consisted of a two-hour thermal cycle between –50°C and 95°C with 15-20 minute dwells at the extreme temperatures. Electrical functionality was verified at one-week intervals using existing production equipment. Modules that passed the functional test were returned to the temperature testing chambers, while failed modules were subjected to root-cause analysis. Repairable modules were fixed and returned to the temperature chamber. In addition to the temperature tests, modules were subjected to ten hours of random vibration at 6.10 G_{rms}. The modules where not powered during the vibration test.

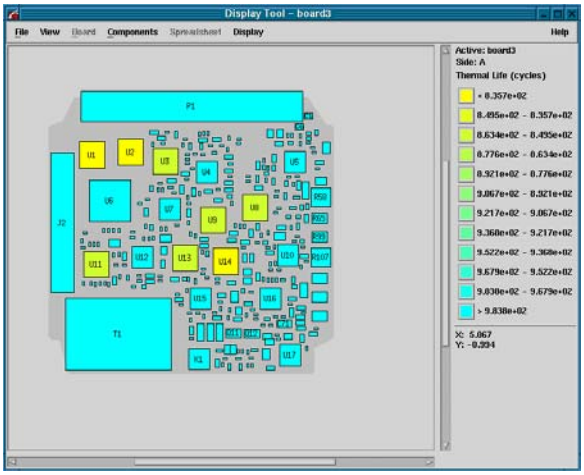


Figure 9 Thermal Fatigue Failures for CCA#3

Ten modules containing the three CCAs were used in the physical tests. No failures occurred during the vibration tests. For the thermal tests, the ten modules averaged slightly over 2000 hours. Observed failures included solder joint failure of ceramic leadless chip carriers (LCC), failure of a electrical coils due to conformal coating, shorting of voltage regulator due to manufacturing defects, lead failure of connectors due to thermal cycling, device failure of a hybrid, and solder-joint failure of a J-leaded device. Of the precipitated failures, the LCC solder joint fatigue was clearly the dominant failure mechanism. The mean-cycles to failure for the LCC's were 967 compared to the predicted value of 900 hours (Ref. 10). The other failure mechanisms were isolated incidents

associated with manufacturing problems.

4. *COST SAVING FROM THIS ANALYSIS*

A design change was implemented in this military radio which eliminated the LCC from the control module. By eliminating these premature failures from the military radio's design, a potential of 90,000 circuit card repairs were avoided during the expected 20 year lifetime of the 5,000 radios to be fielded. The repair, transportation, inventory, and logistics costs associated with these 90,000 circuit card repairs was estimated to be $27M (Grove et al, 1998). By performing this failure assessment on the control model and eliminating the dominant failure mechanism, $27M in cost to the U.S. military was avoided. In addition to the significant cost savings, the availability of these radios was greatly increased.

5. *SUMMARY*

The application of failure assessment software for electronic products can highlight design flaws and significantly reduce the cost of product ownership. Key features of failure assessment software include: product modeling, stress assessment, failure model evaluation, and display. The analysis process is supported with design databases which includes materials, electronic structures, environmental/usage profiles and failure models. To fit in the design process, the failure assessment software must have a high level of information sharing between electrical and mechanical design tools. Even the EDA is now realizing this need (Ref 3.). Furthermore, to achieve the maximum impact, failure assessment must be employed early in the design process and carried into the detailed design stage. The calcePWA software has been shown as an example of a failure assessment software package for circuit card assemblies.

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