

Effect of ENEPIG Surface Finish on the Vibration Reliability of Solder Interconnects

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Abstract

Surface finishes are used to preserve and promote solderability of exposed copper metallization on printed wiring boards. While in the best of worlds, the solder used in assembly should dictate the solder interconnect reliability, surface finishes are known to have an effect. The effect of surface finishes on solder interconnect reliability can be particularly strong under high strain rate loading conditions. In this study, durability of solder interconnects formed between BGAs and electroless nickel, electroless palladium, immersion gold (ENEPIG) finished pads assembled using SnPb and SAC305 solders under harmonic vibration loading is examined. ENEPIG test specimens with two thicknesses of palladium were evaluated. Isothermal preconditioning levels at 100°C for 24 hrs and 500 hrs were included to evaluate the impact of intermetallic evolution on the durability of the soldered interconnects. For comparison, tests specimens created with immersion silver (ImAg) finished printed wiring boards were also included. The failure data obtained found the durability of interconnects formed with ENEPIG finish was comparable or better durability than the durability of interconnects formed with ImAg finish irrespective of the solder. The tests indicate that the use of a thicker palladium layer reduced the degradation in durability which occurred from isothermal aging.

Key words

Lead Free Electronics, BGA Packages, Solder Interconnects, Reliability, Surface Finish, ENEPIG.

I. Introduction

The electronics industry continues to advance manufacturing and packaging technologies to meet the consumer demands for faster, cheaper and smaller electronic products. As a consequence, the use of higher density packages such as chip-scale package (CSP), ball-grid array (BGA) and flip-chip ball-grid array (FC-BGA) have gained popularity over more conventional packages, such as the thin small outline package (TSOP) or the quad-flat-pack package (QFP). However, with the smaller, stiffer interconnects there has been an increased concern regarding the interconnect reliability under high strain rate loading conditions (vibration and drop) [1][2]. Under high strain rate loading, failure of solder interconnects often originates in the interfacial intermetallic compound (IMC) layers, formed between the solder and terminal substrate [1][3][4]. The composition and morphology of interfacial IMC layer is governed by many factors including original surface finish on the terminal substrate, reflow temperature, solder composition, and aging condition. Of these factors, the

surface finish used on the printed circuit board (PCB) terminal pads is often the easiest to control.

A wide variety of PCB surface finishes are currently available, including immersion tin (ImSn), immersion silver (ImAg), Organic Solderability Preservatives (OSP), and electroless nickel/ immersion gold (ENIG). Among these finishes, ENIG has been the most widely used surface finish for high reliability applications [4][5][6][7]. The electroless plating process involved in the ENIG surface finish also makes it conducive for increasing miniaturization seen in electronic products [8][9]. However, the ENIG surface finished solder interconnects are susceptible “Black Pad”, the formation Ni(P) corrosion that can occur during the immersion gold plating operation and results in compromised interconnect reliability [7][10][11]. Further, the porosity of the gold which is very thin (<5 micro-inches) can result in pitting corrosion prior to assembly which may also compromise interconnect reliability [12]. Electroless nickel/electroless palladium/ immersion gold (ENEPIG) surface finish avoids both the black pad and corrosion issue.

For this finish, the palladium layer acts as a protective layer over the nickel layer eliminating the Ni(P) potential corrosion during the gold plating process and corrosion of the nickel due to porous gold in storage [7][8][10][14].

As a relatively new finish, ENEPIG initially was widely rejected due to concerns with compatibility with eutectic SnPb solders [15]. It has, however, gained recent attention in industry due to new RoHS requirements forcing many companies to use solders containing no lead. Past studies have primarily focused on wire-bonding to ENEPIG finished boards and components. No studies have been reported on the vibration interconnect durability of packages assembled on ENEPIG finished boards. Furthermore, there is no consensus regarding how the thickness of the palladium layer impacts the reliability of the solder interconnects.

In this study, the vibration durability of solder interconnects fabricated on ENEPIG finished printed wiring boards with two palladium thickness were examined. For the tests, a eutectic SnPb solder and a SAC305 solder are used. Tests include specimens that were preconditioned at 100°C for either 24 hours or 500 hours. Isothermal aging results in changes in the interfacial and bulk intermetallic compounds (IMCs) as well as the bulk grain structure which in turn affects the reliability of the solder interconnect [16][17][18]. The data obtained from this study provides insight into the role of palladium thickness on the long term vibration reliability of solder interconnects. The failure data obtained from these boards were also compared to failure data obtained from immersion silver (ImAg) boards subject to the identical testing conditions. Details regarding the test boards and experimental setup, as well as a discussion of the results are provided in the following sections.

II. Experimental Setup and Testing Procedure

For this study, a test vehicle (see Figure 1) comprised of a four layer 9"x4.5"x0.062" board made from a Polyclad 370HR laminate was used. Sets of test specimens were created with one of the three surface finishes listed in Table 1. Each test board was populated with four 192 I/O Ceramic Array Ball Grid Array (CABGA) packages. Both SnPb and SAC305 test specimens were created. For these test specimens, the solder paste matched the solder composition of solder spheres on the CABGA packages. For each the CABGA package, the solder spheres were laid out on a 16 by 16 array at a 0.8 mm pitch with the center 8 by 8 positions unpopulated. Each solder sphere had an original diameter of approximately 0.46 mm.

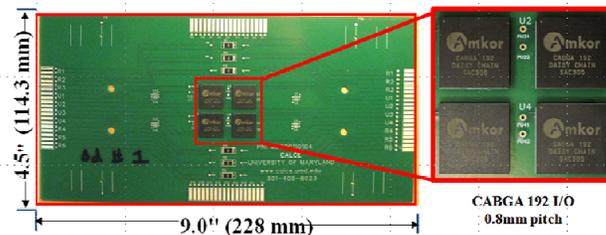


Figure 1: Test Vehicle

Table 1: Test Vehicle Surface Finish

Surface Finish	Material	Thickness
ImAg	Silver (Ag)	0.2 μm
ENEPIG-A	Nickel (Ni)	5 μm
	Palladium (Pd)	0.05 μm - 0.10 μm
	Gold (Au)	30 nm - 50 nm
ENEPIG-B	Nickel (Ni)	5 μm
	Palladium (Pd)	0.15 μm - 0.20 μm
	Gold (Au)	30 nm - 50 nm

Thermal aging (preconditioning) of the test boards was performed at 100°C. Table 2 provides details regarding the test plan and sample size (number of boards) used in this study. The extended aging condition (500 hours) allows for changes to the interconnection microstructure, such as increased interfacial IMC thickness, that provides insight into the long term reliability of the solder interconnects formed on the three surface finishes used in the study.

Table 2: Test Plan and Sample Size (No. of Boards)

Solder Type	SnPb	
	100°C/24 hrs	100°C/500 hrs
ImAg	4	4
ENEPIG-A	4	4
ENEPIG-B	4	4

(a)

Solder Type	SAC305	
	100°C/24 hrs	100°C/500 hrs
ImAg	4	4
ENEPIG-A	4	4
ENEPIG-B	4	4

(b)

After isothermal aging, test boards were subjected to harmonic uni-directional vibration at acceleration level of 3G on the fixture. For this test condition, each test board was clamped in a test fixture across its narrower width at

both ends as shown schematically in Figure 2. In this arrangement, the BGAs were centered on a 6 inch unsupported span. As fixture, the resonant frequency of the test boards was found to be between 192 and 201 Hz. Accelerometers attached on the test boards were used to measure and monitor the board acceleration levels during the test. At the resonant frequency of the test board, a transmissibility of approximately 30 times the base acceleration input measured at the fixture was recorded for the boards.

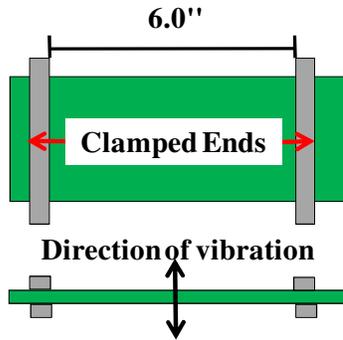
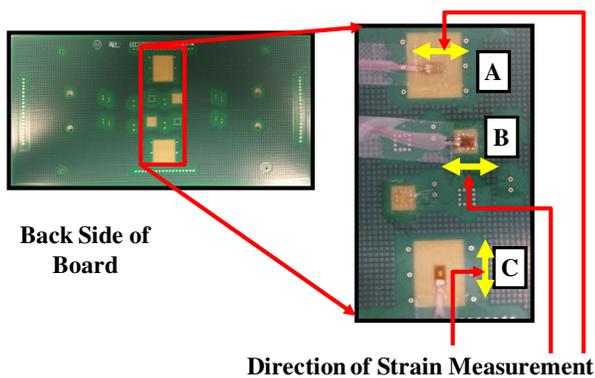
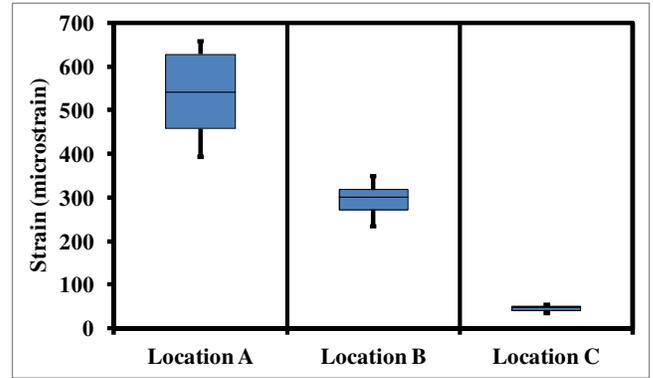


Figure 2: Schematic of Test Setup

In addition to acceleration, board strain was monitored using three strain gages mounted to the printed wiring board (PWB) as shown in Figure 3 (a). The strain gages were attached with epoxy to regions with no solder mask on the unpopulated side of the board. Two strain gages (A & B) were oriented to detect strain perpendicular to the clamped supports with 'A' along the center of the board and 'B' under a BGA part. A third strain gage (C) was also placed along the center of the board but oriented to detect strain parallel to the directions of the clamp supports. Figure 3 (b) provides a box plot of the measured strain at the three locations over all tests. As seen in the Figure 3, the strain experienced under the BGA packages (Location B) were approximately 300 μ strain across all test vehicles. Based on the symmetry of the design and fixture, this strain level is assumed to be the same for all BGAs on each board.



(a)



(b)

Figure 3: (a) Strain Measurement Locations; (b) Measured Strain

Resistance monitoring was carried out during each test for low resistance paths formed for each component on each test board to determine time to failure. Failure is defined based on the IPC-9701 standard, which defines failure as a 20% increase in initial resistance value for five consecutive scans.

III. Results and Failure Analysis

The cycles to failure were estimated by multiplying the time to failure with the measured cyclic frequency. The cycles to failure data were fit to 2-Parameter Weibull distributions to obtain characteristic life (η) and shape parameter (β). These Weibull results are tabulated in Table 3. As is seen from these results, the shape parameters in all but two cases are less than 1. In the case of the SnPb solder, the characteristic lives for the ImAg and the ENEPIG samples were similar. However, in the case of the SAC305 solder, the characteristic lives of the ENEPIG samples exceed those of the ImAg samples.

Table 3: Weibull parameters (a) SnPb Solder (b) SAC305 Solder

Solder Type	SnPb			
	100°C/24 hrs		100°C/500 hrs	
Weibull Parameters	η	β	η	β
ImAg	2.4E+06	0.7	4.9E+06	0.7
ENEPIG-A	5.6E+06	0.8	1.0E+06	1.0
ENEPIG-B	6.7E+06	0.6	2.1E+06	1.3

(a)

Solder Type	SAC305			
Aging Condition	100°C/24 hrs		100°C/500 hrs	
Weibull Parameters	η	β	η	β
ImAg	6.2E+05	0.7	5.8E+05	0.5
ENEPIG-A	2.4E+07	0.8	3.8E+06	0.6
ENEPIG-B	1.0E+07	0.8	3.5E+06	0.6

(b)

Figure 4 provides graphic of the measured characteristic lives comparing isothermal aging state for SnPb and SAC samples. From these plots, the characteristic lives of the ImAg samples are not found to be degraded by isothermal aging. However, the characteristic lives of the ENEPIG samples are found to decrease with isothermal aging. Similar results have also been reported for interconnects formed with nickel-tin interfacial IMC subjected to temperature cycling in literature [15]. This drop may be due to the gold or palladium impacting the formation of the interfacial IMC layer and changes to the bulk solder. The drop in characteristic life with increased aging durations was more significant in the ENEPIG finish with the thinner palladium layer.

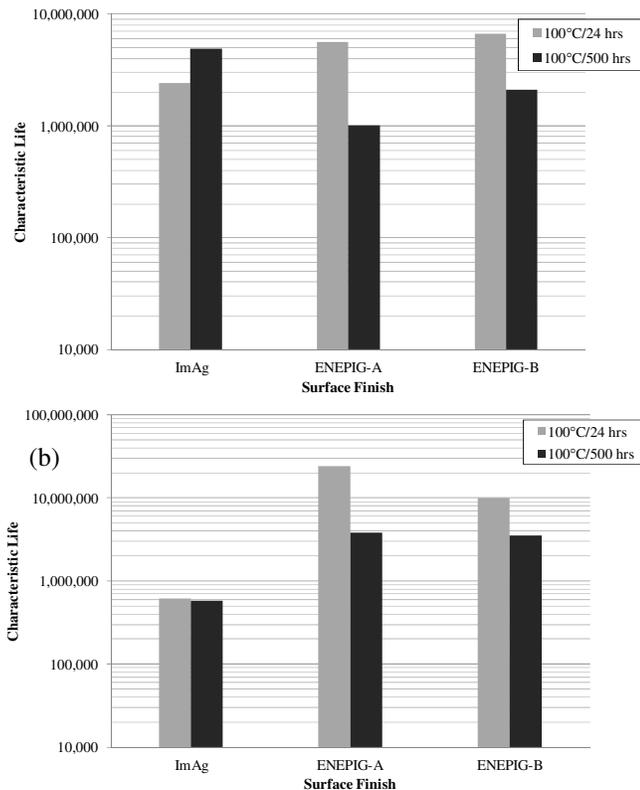


Figure 4: Impact of Aging (a) SnPb Solder (b) SAC305 Solder

Failure analysis was performed on test specimens to isolate the site of failure. Figure 5 shows E-SEM images of

a typical failed solder interconnect. Solder cracks were observed at the component side near the solder-component interfaces. Similar component side failures were obtained across all test configurations. This behavior can be attributed to the solder geometry. The solder mask pad definition of the solder balls at the solder-component interface results in a necking of the solder ball which elevates the stress and strain in the solder on the component side of the interconnect.

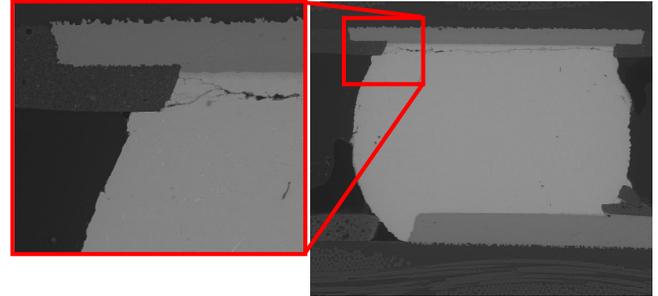


Figure 5: Cross-section of failed sample - ENEPIG - A (SAC305 Solder, 500 hrs Aged @ 100°C)

IV. Conclusions

In this study, the impact of the ENEPIG surface finish on the board level vibration durability was investigated. From the results of this study, the SnPb solder interconnects formed with the ENEPIG finished boards showed similar reliability to the ImAg finished boards. However, in case of the SAC305 solder, the ENEPIG finished boards outperformed the ImAg finished boards. The failure of the solder interconnects were all on the component side owing to solder geometry. It was also noted that an increased aging duration also resulted in a decrease in characteristic life for the ENEPIG finished boards. This result may be due to the palladium changing the interfacial IMCs and bulk solder microstructure. This suggestion is based on the observation that samples with the thicker palladium experienced lower degradation in characteristic life compared with samples created with the ENEPIG finish with the thinner palladium thickness. However, a review of the test results indicated that the ENEPIG finish can provide interconnects that are reliable under vibration loads.

References

- [1] T. You, Y. Kim, W. Jung, J. Moon, and H. Choe, "Effect of surface finish on the fracture behavior of Sn–Ag–Cu solder joints during high-strain rate loading," *Journal of Alloys and Compounds*, Vol. 486, pp 242-245, 2009.
- [2] F. Ferdinandi, "Introduction of a New PCB Surface Finish for the Electronics Industry", *Proceedings of the SMTA International*, 2009.
- [3] P. Liu, P. Yao and J. Liu, "Effects of multiple reflows on interfacial reaction and shear strength of SnAgCu

- and SnPb solder joints with different PCB surface finishes,” *Journal of Alloys and Compounds*, Vol. 470, pp 188-194, 2009.
- [4] A. Sharif, M. N. Islam, and Y.C. Chan, “Interfacial reactions of BGA Sn–3.5%Ag–0.5%Cu and Sn–3.5%Ag solders during high-temperature aging with Ni/Au metallization,” *Materials Science and Engineering B*, Vol. 113 pp 184–189, 2004.
- [5] A. Bansal, S. Yoon, J. Xie, Y. Li and V. Mahadev, “Comparison of Substrate Finishes for Flip Chip Packages,” *Proceedings of the Electronic Components and Technology Conference*, pp 30-37, 2005.
- [6] Y. D. Jeon, Y. B. Lee, and Y. S. Choi, “Thin Electroless Cu/OSP on Electroless Ni as a Novel Surface Finish for Flip Chip Solder Joints” *Proceedings of the Electronic Components and Technology Conference*, pp 119-124, 2006.
- [7] W. H. Wu, C. S. Lin, S. H. Huang, and C. E. Ho “Influence of Palladium Thickness on the Soldering Reactions Between Sn-3Ag-0.5Cu and Au/Pd(P)/Ni(P) Surface Finish,” *Journal of Electronic Materials*, Vol. 39, No. 11, pp 2387-2396.
- [8] C. H. Fu, L. Y. Hung, D. S. Jiang, C. C Chang, Y. P. Wang, and C. S Hsiao, “Evaluation of New Substrate Surface Finish: Electroless Nickel/Electroless Palladium/Immersion Gold (ENEPIG),” *Proceedings of the Electronic Components and Technology Conference*, pp 1931-1935, 2008.
- [9] Q. V. Bui, N. D. Nam, D. H. Choi, J. B. Lee, C. Y. Lee, A. Kar, J. G. Kim, and S. B. Jung, “Corrosion Protection of ENIG Surface Finishing using Electrochemical Methods,” *Materials Research Bulletin*, Vol. 45, pp 305–308, 2010.
- [10] C. F. Tseng, T. K. Lee, G. Ramakrishna, K. C Liu, and J, G Duh, “Suppressing Ni₃Sn₄ Formation in the Sn–Ag–Cu Solder Joints with Ni–P/Pd/Au Surface Finish,” *Materials Letters*, Vol. 65, pp 3216–3218, 2011.
- [11] K. Zeng, V. Vuorinen, and J. K. Kivilahti “Interfacial Reactions Between Lead-Free SnAgCu Solder and Ni(P) Surface Finish on Printed Circuit Boards,” *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 25, No. 3, pp 162-167, 2002.
- [12] J.P. Le Solleu “Sliding Contacts on Printed Circuit Boards and Wear Behavior,” *The European Physics Journal of Applied Physics*, Vol. 50, Issue 1, pp 12902 p1-p6, 2010.
- [13] Y. Xia, and X. Xie, “Endurance of Lead-free Assembly under Board Level Drop Test and Thermal Cycling,” *Journal of Alloys and Compounds*, Vol. 457, pp 198-203, 2008.
- [14] W. Johannes, P. Vianco, J. Rejent, B. McKenzie, “Long Term Reliability of Eutectic Sn-Pb and Pb-Free Solder Joints Made to the ENEPIG Surface Finish,” *Proceedings of the SMTA International*, 2012.
- [15] C. W. W. Ng, B. C. Marbella, and L. K. I. Koh, “Evaluation of ENEPIG Substrate for Handheld Product Application,” 2009 11th Electronics Packaging Technology Conference, Singapore, 2009.
- [16] T. K Lee, H. Ma, K. C. Liu and J. Xue, “Impact of Isothermal Aging on Long-Term Reliability of Fine-Pitch Ball Grid Array Packages with Sn-Ag-Cu Solder Interconnects: Surface Finish Effects,” *Journal of Electronic Materials*, Vol. 39, No. 12, pp 2564-2573, 2010.
- [17] J. H. L. Pang, T. H. Low, B. S. Xong, X. Luhua, and C. C. Neo, “Thermal Cycling Aging Effects on Sn–Ag–Cu Solder Joint Microstructure, IMC and Strength,” *Thin Solid Films* Vol. 462–463, pp 370– 375, 2004.
- [18] J. H. L. Pang, X. Luhua, X.Q. Shi, W. Zhou, and S.L. Ngho “Intermetallic Growth Studies on Sn-Ag-Cu Lead-Free Solder Joints” *Journal of Electronic Materials*, Vol. 33, No. 10, 2004